What Is Claimed Is:

1. An array substrate for a liquid crystal display device, comprising:

a transparent substrate;

a gate line arranged along a first direction on the transparent substrate;

a gate electrode extending from the gate line;

a common line arranged along the first direction adjacent to the gate line and having a protrusion;

a gate insulation layer on the transparent substrate to cover the gate line, the gate electrode, and the common electrode;

an active layer on the gate insulation layer and over the gate electrode;

first and second ohmic contact layers on the active layer;

a data line arranged along a second direction perpendicular to the first upon the gate insulation layer;

a source electrode extending from the data line and contacting the first ohmic contact layer;

a drain electrode spaced apart from the source electrode and contacting the second ohmic contact layer;

a first capacitor electrode formed on the gate insulation layer and connected to the drain electrode, the first capacitor electrode overlapping the common line and the protrusion of the common line;

a passivation layer formed on the gate insulation layer to cover the data line, the source and drain electrodes, and the first capacitor electrode, the passivation layer having a first contact hole exposing a portion of the capacitor electrode; and

a pixel electrode formed on the passivation layer and contacting the first capacitor electrode through the first contact hole.

2. The array substrate according to claim 1, wherein the common line includes a same material as the gate line.

3. The array substrate according to claim 2, wherein the common line and the gate line include an opaque metallic material.

4. The array substrate according to claim 1, wherein the data line, the source and drain electrodes, and the first capacitor electrode are simultaneously formed of a same material.

5. The array substrate according to claim 1, further comprising a second capacitor electrode formed upon the gate insulation layer and covers a portion of the gate line.

6. The array substrate according to claim 5, wherein the first capacitor electrode and the second capacitor electrode are simultaneously formed of a same material.

7. The array substrate according to claim 5, wherein the passivation layer includes a second contact hole exposing a portion of the second capacitor electrode.

8. The array substrate according to claim 7, wherein the pixel electrode contacts the second capacitor electrode through the second contact hole.

9. The array substrate according to claim 1, wherein the protrusion extends from the common line toward the gate line along the second direction.

10. The array substrate according to claim 9, wherein the protrusion is arranged between the gate line and the common line.

11. The array substrate according to claim 1, wherein the gate line and the data line define a pixel region.

12. The array substrate according to claim 12, wherein the pixel electrode is disposed within the pixel region.

13. A liquid crystal display device, comprising:

a first transparent substrate;

a second transparent substrate facing the first transparent substrate;

a gate line arranged on the first transparent substrate along a first direction;

a data line arranged on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

a thin film transistor arranged on the first transparent substrate and adjacent to the pixel region, the thin film transistor electrically connected to both the gate line and the data line;

a common line arranged on the first transparent substrate along the first direction parallel with and adjacent to the gate line, the common line having a protrusion;

a first capacitor electrode overlapping a portion of the common line and the protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor;

a pixel electrode formed within the pixel region, the pixel electrode contacting the first capacitor electrode;

a black matrix on the second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and common line; and

a common electrode on the second transparent substrate to cover the black matrix.

14. The device according to claim 13, wherein the common line includes a same material as the gate line.

15. The device according to claim 14, wherein the common line and the gate line are simultaneously formed of an opaque metallic material.

16. The device according to claim 13, wherein the data line and the first capacitor electrode are simultaneously formed of a same material.

17. The device according to claim 13, further comprising a second capacitor electrode overlapping a portion of the gate line to form a second storage capacitor.

18. The device according to claim 17, wherein the first capacitor electrode and the second capacitor electrode are simultaneously formed of a same material.

19. The device according to claim 17, wherein the second capacitor electrode is electrically connected to the pixel electrode.

20. The device according to claim 13, wherein the protrusion extends from the common line toward the gate line along the second direction.

21. The device according to claim 20, wherein the protrusion is arranged between the gate line and the common line.

22. A method for fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a gate line arranged along a first direction on a transparent substrate;

forming a gate electrode extending from the gate line;

forming a common line arranged along the first direction adjacent to the gate line on the transparent substrate and having a protrusion;

forming a gate insulation layer on the transparent substrate to cover the gate line, the gate electrode, and the common electrode;

forming an active layer on the gate insulation layer and over the gate electrode;

forming first and second ohmic contact layers on the active layer;

forming a data line arranged along a second direction perpendicular to the first upon the gate insulation layer;

forming a source electrode extending from the data line and contacting the first ohmic contact layer;

forming a drain electrode spaced apart from the source electrode and contacting the second ohmic contact layer;

forming a first capacitor electrode on the gate insulation layer to connect to the drain electrode, the first capacitor electrode overlapping the common line and the protrusion of the common line;

forming a passivation layer on the gate insulation layer to cover the data line, the source and drain electrodes, and the first capacitor electrode, the passivation layer having a first contact hole exposing a portion of the capacitor electrode; and

forming a pixel electrode on the passivation layer to contact the first capacitor electrode through the first contact hole.

23. The method according to claim 22, wherein the common line includes a same material as the gate line.

24. The method according to claim 23, wherein the common line and the gate line include an opaque metallic material.

25. The method according to claim 22, wherein the steps of forming the data line, the source and drain electrodes, and the first capacitor electrode are simultaneously formed of a same material.

26. The method according to claim 22, further comprising a step of forming a second capacitor electrode on the gate insulation layer to cover a portion of the gate line.

27. The method according to claim 26, wherein the step of forming a first capacitor electrode and the step of forming a second capacitor electrode are simultaneously performed using a same material.

28. The method according to claim 26, wherein the step of forming a passivation layer includes forming a second contact hole to expose a portion of the second capacitor electrode.

29. The method according to claim 28, wherein the pixel electrode contacts the second capacitor electrode through the second contact hole.

30. The method according to claim 22, wherein the protrusion extends from the common line toward the gate line along the second direction.

31. The method according to claim 30, wherein the protrusion is arranged between the gate line and the common line.

32. The method according to claim 22, wherein the gate line and the data line define a pixel region.

33. The method according to claim 32, wherein the pixel electrode is disposed within the pixel region.

34. A method for fabricating a liquid crystal display device, comprising the steps of:

forming a gate line on a first transparent substrate along a first direction;

forming a data line on the first transparent substrate along a second direction perpendicular to the first direction, the gate line and the data line perpendicularly crossing each other and defining a pixel region;

forming a thin film transistor on the first transparent substrate and adjacent to the pixel region, the thin film transistor is electrically connected to both the gate line and the data line;

forming a common line on the first transparent substrate along the first direction parallel with and adjacent to the gate line, the common line having a protrusion;

forming a first capacitor electrode to overlap a portion of the common line and the protrusion of the common line to form a first storage capacitor, the first capacitor electrode connected to the thin film transistor;

forming a pixel electrode within the pixel region, the pixel electrode contacting the first capacitor electrode;

forming a black matrix on a second transparent substrate, the black matrix covering the thin film transistor, the protrusion of the common line, and portions of the gate line and common line;

forming a common electrode on the second transparent substrate to cover the black matrix; and

forming the first substrate to face the second substrate.

35. The method according to claim 34, wherein the common line includes a same material as the gate line.

36. The method according to claim 35, wherein the common line and the gate line are simultaneously formed of an opaque metallic material.

37. The method according to claim 34, wherein the steps of forming the data line and the first capacitor electrode are simultaneously formed of a same material.

38. The method according to claim 34, further comprising a step of forming a second capacitor electrode to overlap a portion of the gate line to form a second storage capacitor.

39. The method according to claim 38, wherein the step of forming a first capacitor electrode and the step of forming a second capacitor electrode are simultaneously performed using a same material.

40. The method according to claim 38, wherein the second capacitor electrode is electrically connected to the pixel electrode.

41. The method according to claim 34, wherein the protrusion extends from the common line toward the gate line along the second direction.

42. The method according to claim 41, wherein the protrusion is arranged between the gate line and the common line.